WHAT IS CLAIMED IS:

1. An encoder for encoding a data word having a plurality of bits, wherein the data word is transmittable in parallel on a data bus, wherein for each bit a bus line is provided and wherein each bit may have one of two states, comprising:

a means for examining the data word in order to determine whether a first number of bits of the data word with a first logical state or a second number of bits of the data word with a second logical state exceeds a predetermined threshold, the predetermined threshold being a value that is higher than two thirds of the total number of bits of the data word;

a means for changing the state of a bit of the data word from the number of bits exceeding the predetermined threshold in order to create an encoded data word if the predetermined threshold is exceeded by the data word; and

a means for creating auxiliary information referring to the changed bit.

2. The encoder according to claim 1, wherein the predetermined threshold is a preset ratio between the first number of bits of the data word having a first logical state and the second number of bits of the data word having a second logical state.

3. The encoder according to claim 1, wherein the two states that each bit of a data word may have are complementary logical states.

4. The encoder according to claim 1, wherein the encoder is connectable to a data bus.

5. The encoder according to claim 1, wherein for each bus line of the data bus a driver means is provided.

6. The encoder according to claim 1, wherein the means for examining the data word is a comparator means which compares the logical states of the data word.

7. The encoder according to claim 1, wherein the encoder comprises an inverter means in order to change the state of a bit of the data word.

8. The encoder according to claim 1, wherein the encoder is connectable to a data line in order to transmit the auxiliary information.

9. The encoder according to claim 8, wherein the data line is part of the data bus.

10. The encoder according to claim 1, wherein the encoder is part of an electric device that communicates with a memory device.

11. An encoder for encoding a data word having a plurality of bits, wherein the data word is transmittable in parallel on a data bus, wherein a bus line is provided for each bit and wherein each bit may have one of two logical states, comprising:

a means for comparing the data word to a preceding data word in order to determine whether the number of equal transitions between the two states of each bit of the data word and the preceding data word exceeds a predetermined threshold, the predetermined threshold being chosen to ensure a secure transmission of the data word when the number is below the predetermined threshold;

a means for changing the state of a bit of the data word from the number of bits of the data word, due to which the predetermined threshold is exceeded, in order to create an encoded data word if the predetermined threshold is exceeded by the data word; and

a means for creating auxiliary information referring to the changed bit.

12. The encoder according to claim 11, wherein the predetermined threshold is a preset ratio between the first number of bits of the data word having a first logical state and the second number of bits of the data word having a second logical state.

13. The encoder according to claim 11, wherein the means for comparing the data word to a preceding data word evaluates the number of transitions from one state to the other.

14. The encoder according to claim 11, wherein the two states each bit of a data word may have complementary states.

15. The encoder according to claim 11, wherein the encoder is connectable to a data bus.

16. The encoder according to claim 11, wherein a driver means is provided for each bus line of the data bus.

17. The encoder according to claim 11, wherein the encoder comprises an inverter means in order to change the state of a bit of the data word.

18. The encoder according to claim 11, wherein the encoder is connectable to a data line in order to transmit the auxiliary information.

19. The encoder according to claim 18, wherein the data line is part of the data bus.

20. The encoder according to claim 11, wherein the auxiliary information is encoded into the encoded data word.

21. The encoder according to claim 11, wherein the encoder is part of an electric device communicating with a memory device.

22. An encoder for encoding a data word having a plurality of bits, wherein the data word is transmittable in parallel on a data bus, wherein for each bit a bus line is provided and wherein each bit may have one of two states, the encoder comprising:

a comparator including a plurality of inputs coupled to data lines to receive bits of the data word, the comparator also including an output for carrying a signal based upon a relationship of logical values of the bits of the data word;

a plurality of programmable inverters, each inverter having an input coupled to one of the data lines and a control input coupled to the output of the comparator; and

a plurality of output drivers, a first set of the output drivers having inputs coupled to the data lines and the remainder of the output drivers having inputs coupled to outputs of the programmable inverters.

23. The encoder of claim 22 wherein the output of the comparator is for carrying a signal based on a determination of whether a first number of bits of the data word with a first logical state or a second number of bits of the data word with a second logical state exceeds a predetermined threshold, the predetermined threshold being a value that is higher than two thirds of the total number of bits of the data word.

24. The encoder of claim 22 wherein the output of the comparator is for carrying a signal based on a comparison of the data word to a preceding data word that determines whether the number of equal transitions between the two states of each bit of the data word and the preceding data word exceeds a predetermined threshold.

25. The encoder of claim 24 wherein the predetermined threshold is chosen to ensure a secure transmission of the data word when the number is below the predetermined threshold.

26. A method for encoding a data word having a plurality of bits, wherein the data word is transmittable in parallel on a data bus, wherein a bus line is provided for each bit and wherein each bit may have one of two states, comprising:

examining the data word in order to determine whether a number of bits of the data word having a first logical state or a second number of bits of the data word having a second logical state exceeds a predetermined threshold, the predetermined threshold having a value, which is higher than two thirds of the total number of bits of the data word;

changing the state of a bit of the data word from the number of bits exceeding the predetermined threshold in order to create an encoded data word if the predetermined threshold is exceeded by the data word; and

creating auxiliary information referring to the changed bit.

27. A method for encoding a data word with a plurality of bits, wherein the data word is transmittable in parallel on a data bus, wherein one bus line is provided for each bit and wherein each bit may have one of two logical states, comprising:

comparing the data word to a preceding data word to determine whether the number of equal transitions between the two states of each bit of the data word and the preceding data word exceeds a predetermined threshold, the predetermined threshold being chosen to ensure a secure transmission of the data word when the predetermined threshold is not reached;

changing the state of a bit of the data word from the number of bits of the data word, due to which the predetermined threshold is exceeded, in order to create an encoded data word if the predetermined threshold is exceeded by the data word; and

creating auxiliary information referring to the changed bit.